UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,076	11/13/2001	Craig Nemecek	CYPR-CD01210M	4880

7590 03/17/2006

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,076	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were rejected in office action dated 21 November 2005. Applicants' response has amended claims 2 and 16. Claims 1-20 have been submitted for reconsideration.

Claims 1-20 have been rejected.

Drawings

1. The drawings are objected to because the hand drawn features in FIGS. 2 and 3 are illegible. See 37 CFR 1.83(p). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The previous rejections under 35 U.S.C. § 112, second paragraph, have been withdrawn in light of the amendments to the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 5-11, 13-16, and 18-20 rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,371,878 to Coker.

Regarding claims 1 and 15, Coker discloses a system comprising:

A microcontroller installed on a test circuit, wherein the microcontroller includes a first memory and a first CPU [*"Embedded Computer System (ECS)"* (column 1, line 22); *"FIG. 1 shows the target-ECS 12 connected to the system hardware 16 by a bi-directional bus line 14 allowing communication in either direction between the target-ECS and the system hardware."* (column 4, lines 3-8); FIG. 1, references 12, 12a, 12b, 14, and 16];

An ICE (in circuit emulator) including a second memory and a second CPU [FIG. 1, references 32, 28, 28a, 28b, and 30] coupled to a computer system [FIG. 1, references 34 and 36], wherein the ICE emulates the microcontroller [*"The shadow system 28*

includes and executes the same software and input signals [...] *as the target-ECS 12."* (column 4, lines 40-43); *"The shadow system 28 is connected to an ICE 32 via an electrical connection 30."* (column 4, lines 51-52)] and the microcontroller and the ICE run the microcontroller code in lock step [*"By operating on input data with the same value, memory location and relative timing as the target-ECS, the shadow system has an execution state at any given time corresponding to a known execution state in the target-ECS and can produce a mirror-image or "shadow" of the target-ECS."* (column 3, lines 6-12)];

An interface for coupling the test circuit and the ICE enabling data transmission between the test circuit and the computer system [FIG. 1, references 18, 19, 26, 30, 34, 38, etc.], the computer system configured to compare a content of the first memory against a content of the second memory to verify said lock step (column 3, lines 6-12).

In response, Applicants' argue primarily that (emphasis in original):

> The rejection relies on ICE 32 in order to show ICE (in circuit emulator), as claimed. [...] Independent Claim 1 distinguishes over Coker by reciting the limitation that the ICE emulates the microcontroller. Coker on the other hand fails to show ICE emulating the microcontroller but rather discloses a shadow system 28, which differs from the ICE, emulating the target-ECS 12 by executing the same software and input signals as the target ECS 12. Accordingly, Coker does not disclose ICE emulates the microcontroller, as claimed.

The Examiner respectfully traverses this argument as follows.

Contrary to Applicants' allegations, the rejection does not rely solely on ICE 32 in order to show an in-circuit emulator. Applicants' attention is drawn to the body of the rejection which unambiguously refers to at least references 32, 28, 28a, 28b, and 30 of FIG. 1.

Applicants argue persuasively that shadow system 28 emulates the target-ECS, a fact that was specifically identified in the rejection. The Examiner fails to see how this distinguishes the claimed invention over the prior art. Applicants appear to define patentability based on the terminology used by the applied prior art reference. This is insufficient to establish patentability as expressly stated by MPEP 2131.

Applicants further argue that (emphasis in original):

> Independent Claim 1 distinguishes over Coker by reciting that the ICE runs the microcontroller code in lock step. On the other hand Coker discloses a target-ECS and the shadow system operating on input data with the same value, memory location, and relative timing of one another. Accordingly, Coker does not disclose that the ICE runes the microcontroller code in lock step, as claimed.

The Examiner respectfully traverses this argument as follows.

Coker discloses:

"The shadow system 28 is the same finite state sequential machine as the target-ECS 12. In other words, at any given point in time during execution of the input events, the execution state of the shadow system 28 directly corresponds to the execution state of the target-ECS 12 at the same relative point in time." (column 8, lines 11-16)

"In terms of actual time, the execution states of the shadow system 28 will lag slightly behind that of the target-ECS because of the slight time delay while input events are temporarily stored in the data buffer 24. But in terms of relative time, the execution state of the shadow system 28 at the time when any given instruction is executed will directly correspond to the execution state of the target-ECS 12 when the same instruction was executed." (column 8, lines 41-49)

Applicants have argued persuasively that Coker discloses a target-ECS and a shadow system that operate on input data with the same value, memory location, and relative timing as each other. The Examiner fails to see how this distinguishes the claimed invention over the prior art. Coker clearly explains that the "relative timing" differs from "actual time" because of the latency inherent in computer data communication. Still, this disclosure meets the definition of "lock step," which has no implicit or explicit limitation that the latency inherent in computer data communication is excluded.

Applicants further argue that (emphasis in original):

> Moreover, independent Claim 1 distinguishes over Coker by reciting that the computer system is configured to compare a content of the first memory against a content of the second memory to verify said lock step. [...] The Applicant has found no teaching in Coker suggesting comparison of memories to verify the lock step as claimed. Accordingly, Coker does not disclose the computer system configured to compare a content of the first memory against a content of the second memory to verify said lock step, as claimed.

The Examiner respectfully traverses this argument as follows.

The claim language recites that "the computer system is configured to compare a content of the first memory against a content of the second memory to verify said lock step." The claim language does not recite a step of comparing a content of the first memory against a content of the second memory.

As cited in the rejection, Coker discloses that the shadow system produces a "mirror image or shadow" of the target-ECS (column 3, lines 6-12).

Coker clearly discloses that the target-ECS and shadow system operate in lock step, as shown above.

Coker clearly discloses that lock step execution is achieved by transmitting input events from the I/O registers 12b of the target-ECS 12 to the I/O state memory 28b of the shadow system 28 (column 4, lines 40-49). It is the equivalent memory contents between the I/O registers 12b and the I/O state memory 28b that verifies the lock step execution.

Applicants' arguments amount to the conclusion that Coker's host system 36 is incapable of comparing memory contents, which is not reasonable and not supported by the reference.

Applicants' arguments for claims 2, 5-8, 9-11, 13-14, 15-16, and 18-20 rejected under 35 U.S.C. § 102(b) refer to those arguments addressed above. Applicants' arguments for claims 3, 4, 12, and 17 rejected under 35 U.S.C. § 103(a) refer to those arguments addressed above. In light of the response shown above, no further response is deemed necessary.

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claims 2 and 16, Coker discloses that the microcontroller is installed on an external circuit board [FIG. 1, reference 10].

Regarding claims 5 and 18, Coker discloses that the first and second memory each include a plurality of register files (column 3, lines 6-12).

Regarding claim 6, Coker discloses that lock step execution is maintained by keeping a first and second program counter in lock step [(column 3, lines 6-12); *"Internal state vectors are*

defined as the contents of RAM and internal registers, i.e., interrupt and status registers, of both the target-ECS and the shadow system." (column 8, lines 50-65)].

Regarding claims 7, 8 and 19 Coker discloses that the system supports debugging features, implying to a person of ordinary skill in the art the recited steps (column 4, lines 51-61).

Regarding claims 9-11 and 14, these claims recite methods of using the system of claim 1. Coker discloses the system of claim 1 as shown above, and discloses that the system is used for debugging [*"The ICE 32 is a commercially available system allowing the shadow system 28 to be controlled and debugged."* (column 4, lines 51-61); *"The host system 36 is connected to a permanent storage device 36a capable of storing all data necessary to re-create a real time scenario for debug, verification and development purposes."* (column 9, lines 31-42)]. Coker discloses that lock step execution is maintained by keeping a first and second program counter in lock step [(column 3, lines 6-12); (column 8, lines 50-65)]. Coker discloses saving execution history and a trace buffer (column 3, lines 13-34).

Regarding claims 13 and 20, Coker discloses that the microcontroller is a production microcontroller [*"an ECS normally executes software in which the user interface is implemented as a system interface, e.g., a user interface of a computer controlled microwave oven."* (column 1, lines 29-39)].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker as applied to claim 1 above, and further in view of US Patent No. 6,173,419 to Barnett.

4. Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker as applied to claim 9 above, and further in view of US Patent No. 6,173,419 to Barnett.

5. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker as applied to claim 15 above, and further in view of US Patent No. 6,173,419 to Barnett.

Regarding claims 3, 12 and 17 Coker does not expressly disclose whether the shadow system is implemented using an FPGA.

Barnett teaches an emulation system wherein an FPGA is programmed to emulate a microcontroller (column 5, lines 37-55). Barnett teaches that such a system is advantageous by allowing it to be reconfigured (column 5, lines 31-36).

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the FPGA emulator taught by Barnett with the system of Coker in order to benefit from well-known advantages of hardware emulation, such as speed, as well as the advantages of being reconfigurable, as explicitly taught by Barnett. The combination could be achieved by implementing the shadow system of Coker with an FPGA.

6. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker as applied to claim 1 above, and further in view of "State of the Art" by Stan Augarten, published 1983 (Augarten)

Regarding claim 4, Coker discloses a first and second memory [FIG. 1, references 12a, 12b, 28a, and 28b]. Coker does not expressly disclose whether these memories are static random access memory.

Augarten discloses that SRAM has been known in the art since 1970. Augarten expressly teaches the advantages of SRAM [*"The charges in static RAMs do not leak away, freeing such chips from the need for periodic refreshing"* ... *"this chip was able to retain, in the space of a single core, many times the amount of information"* (third paragraph)]

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use the well-known technology of SRAM when implementing the

system of Coker in order to produce a system having a memory that does not need periodic refreshing and stores many times the amount of information held by traditional ferro-magnetic core memory.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

jsp

Paul L. Rodriguez 3/15/06
Primary Examiner
Art Unit 2125 2125